CLAIMS

1. A digital signal receiving system comprising:

a digital signal receiving device which receives a digital communication signal, has a function of generating a clock signal based on PCR data included in the communication signal, and a function of transmitting a stream signal in the form of a plurality of packets, as well as the clock signal, the stream signal including the communication signal; and

a host device which receives the stream signal and the clock signal from the digital signal receiving device via an interface section,

the digital signal receiving device including:

a recipient STC counter which counts the number of clocks of the clock signal and outputs the counter value as recipient STC data;

a variation detector which calculates a difference between the recipient STC data and the PCR data as difference data, and detects a variation in frequency of the clock signal that exceeds a predetermined value based on the difference data; and

a variation processor which sends, to the host device, variation information data obtained based on the recipient STC data and the PCR data, and sets the PCR data in the recipient STC counter if the variation detector detects the variation in frequency that exceeds the predetermined value, and

the host device including:

a host STC counter which counts the number of clocks of the clock signal sent from the digital signal receiving device, and outputs the counter value as host STC data; and

an STC correcting unit which calculates correction data based on the host STC data and the variation information data if the variation detector detects the variation in frequency that exceeds the predetermined value, and sets the correction data in the host STC counter so as to coincide the counter value set in the recipient STC counter with the counter value set in the host STC counter.

2. The digital signal receiving system according to Claim 1, wherein the variation information data is a value that has been accumulated since the variation has been detected for the first time, the digital signal receiving device further includes a counter section which counts the number of times of variation detection from the first time of variation detection, and the host device further includes a judging unit which accumulatively stores the number of times of variation detection sent from the digital signal receiving device one after another, compares the stored number of times of variation detection with the number of times of variation detection which has sent from the digital signal receiving device most lately, and sets the variation information data as the correction data

if the stored number of times of variation detection and the latest number of times of variation detection are not serial integers.

3. The digital signal receiving system according to Claim 1 or 2, wherein the STC correcting unit calculates a difference between the PCR data and the recipient STC data, performs a predetermined calculation based on the difference and the host STC data, and sets the calculation result in the host STC counter as the correction data, the PCR data and the recipient STC data being supplied as the variation information data.

4. The digital signal receiving system according to Claim 3, wherein the STC correcting unit calculates a difference by subtracting the recipient STC data from the PCR data, performs the calculation by adding the difference to the host STC data, and sets the calculation result in the host STC counter as the correction data, the PCR data and the recipient STC data being supplied as the variation information data.

5. The digital signal receiving system according to Claim 1 or 2, wherein the STC correcting unit obtains a difference between the PCR data and the recipient STC data, performs a predetermined calculation based on the difference and the host STC data, and sets the calculation result in the

host STC counter as the correction data, the difference between the PCR data and the recipient STC data being supplied as the variation information data.

6. The digital signal receiving system according to Claim 5, wherein the STC correcting unit obtains a difference by subtracting the recipient STC data from the PCR data, performs the calculation by adding the difference to the host STC data, and sets the calculation result in the host STC counter as the correction data, the difference by subtracting the recipient STC data from the PCR data being supplied as the variation information data.

7. The digital signal receiving system according to any one of Claims 3 through 6, wherein the variation information data is transmitted from the digital signal receiving device to the host device via the interface section while being attached to the stream signal.

8. The digital signal receiving system according to Claim 7, wherein the variation detector detects the variation in frequency of the clock signal based on the difference data.

9. The digital signal receiving system according to Claim 8, wherein the variation detector outputs a variation detection signal indicative of the detection of the variation

in frequency of the clock signal if the difference data is out of a range defined by a predetermined lower limit and a predetermined upper limit.

10. The digital signal receiving system according to Claim 9, wherein the digital signal receiving device further includes an additive information attaching unit which sets a flag indicating whether the variation information data is valid, and attaches additive information including the flag and the variation information data to the stream signal.

11. The digital signal receiving system according to Claim 10, wherein the host device further includes an additive information extracting unit which extracts the additive information attached to the stream signal, and supplies the variation information data extracted from the additive information to the STC correcting unit, the stream signal being sent from the digital signal receiving device to the host device via the interface section.

12. The digital signal receiving system according to Claim 11, wherein the digital signal receiving device further includes a command receiving unit which receives, from the host device, command data for controlling respective processing in the digital signal receiving device, and a notification unit which notifies the host device of information sent from the

digital signal receiving device, and the host device further includes a command sending unit which sends, to the digital signal receiving device, the command data for controlling the respective processing in the digital signal receiving device, and a notification receiving unit which receives the information sent from the digital signal receiving device.

13. The digital signal receiving system according to Claim 12, wherein the digital signal receiving device further includes a reset processing unit which resets the recipient STC counter to a predetermined initial state in response to receiving a reset signal sent from the host device via the command receiving unit, and outputs, to the host device, the reset signal indicative of the resetting, and the host device further includes a reset receiving unit which resets the host STC counter to the predetermined initial state based on the reset signal sent from the reset processing unit.

14. The digital signal receiving system according to any one of Claims 1 through 13, wherein the digital signal receiving device and the host device are interconnected with each other via a digital interface.

15. The digital signal receiving system according to Claim 14, wherein at least the stream signal, the clock signal, and the variation information data are transmitted via the

digital interface.

16. The digital signal receiving system according to any one of Claims 1 through 15, wherein the digital signal receiving device is formed as an electronic card.

17. The digital signal receiving system according to Claim 16, wherein the electronic card is configured as an SD card.

18. The digital signal receiving system according to Claim 17, wherein at least the stream signal, the clock signal, and the variation information data are transmitted through a data line defined in compliance with the specifications of the SD card from the SD card as the digital signal receiving device.

19. A digital signal receiving device which is adapted to receive a digital communication signal, has a function of generating a clock signal based on PCR data included in the communication signal, and has a function of transmitting a stream signal in the form of a plurality of packets, as well as the clock signal, the stream signal including the communication signal, the digital signal receiving device being configured so as to establish a digital signal receiving system by being interconnected via an interface section to a host device which is adapted to receive the stream signal and the clock signal

from the digital signal receiving device via the interface section, the digital signal receiving device comprising:

a recipient STC counter which counts the number of clocks of the clock signal, and outputs the counter value as recipient STC data;

a variation detector which calculates a difference between the recipient STC data and the PCR data as difference data, and detects a variation in frequency of the clock signal that exceeds a predetermined value based on the difference data; and

a variation processor which sends, to the host device, variation information data obtained based on the recipient STC data and the PCR data, and sets the PCR data in the recipient STC counter if the variation detector detects that the variation in frequency that exceeds the predetermined value.

20. The digital signal receiving device according to Claim 19, wherein the variation information data includes the recipient STC data and the PCR data.

21. The digital signal receiving device according to Claim 19, wherein the variation information data includes a difference between the PCR data and the recipient STC data.

22. The digital signal receiving device according to Claim 20 or 21, wherein the variation information data is

transmitted from the digital signal receiving device to the host device via the interface section while being attached to the stream signal.

23. The digital signal receiving device according to Claim 22, wherein the variation detector detects the variation in frequency of the clock signal based on the difference data.

24. The digital signal receiving device according to Claim 23, wherein the variation detector outputs a variation detection signal indicative of the detection of the variation in frequency of the clock signal if the difference data is out of a range defined by a predetermined lower limit and a predetermined upper limit.

25. The digital signal receiving device according to Claim 23, wherein the variation detector outputs a variation detection signal indicative of the detection of the variation in frequency of the clock signal if the absolute value of the difference data exceeds a predetermined upper limit.

26. The digital signal receiving device according to Claim 24 or 25, further comprising an additive information attaching unit which sets a flag indicating whether the variation information data is valid, and attaches additive information including the flag and the variation information

data to the stream signal.

27. The digital signal receiving device according to Claim 26, further comprising a command receiving unit which receives, from the host device, command data for controlling respective processing in the digital signal receiving device, and a notification unit which notifies the host device of information sent from the digital signal receiving device.

28. The digital signal receiving device according to Claim 27, further comprising a reset processing unit which resets the recipient STC counter to a predetermined initial state, and outputs, to the host device, the reset signal indicative of the resetting.

29. The digital signal receiving device according to Claim 28, wherein the digital signal receiving device is connectable with the host device via a digital interface in such a manner that at least the stream signal, the clock signal, and the variation information data are transmitted from the digital signal receiving device to the host device via the digital interface.

30. The digital signal receiving device according to any one of Claims 19 through 29, wherein the digital signal receiving device is formed as an electronic card.

31. The digital signal receiving device according to Claim 30, wherein the electronic card is configured as an SD card.

32. The digital signal receiving device according to Claim 31, wherein at least the stream signal, the clock signal, and the variation information data are transmitted through a data line defined in compliance with the specifications of the SD card from the digital signal receiving device.

33. A host device configured so as to establish a digital signal receiving system by being interconnected via an interface section to a digital signal receiving device which is adapted to receive a digital communication signal, has a function of generating a clock signal based on PCR data included in the communication signal, and has a function of sending a stream signal in the form of a plurality of packets, as well as the clock signal, the stream signal including the communication signal, the host device being adapted to receive the stream signal and the clock signal from the digital signal receiving device via the interface section, the host device comprising: a recipient STC counter which counts the number of clocks of the clock signal, and outputs the counter value as recipient STC data; a variation detector which calculates a difference between the recipient STC data and the PCR data as

difference data, and detects a variation in frequency of the clock signal that exceeds a predetermined value based on the difference data; and a variation processor which sends, to the host device, variation information data obtained based on the recipient STC data and the PCR data, and sets the PCR data in the recipient STC counter if the variation detector detects that the variation in frequency that exceeds the predetermined value, the host device comprising:

a host STC counter which counts the number of clocks of the clock signal sent from the digital signal receiving device, and outputs the counter value as host STC data; and

an STC correcting unit which calculates correction data based on the host STC data and the variation information data if the variation detector detects the variation in frequency that exceeds the predetermined value, and sets the correction data in the host STC counter so as to coincide the counter value set in the recipient STC counter with the counter value set in the host STC counter.

34. The host device according to Claim 33, wherein the STC correcting unit calculates a difference between the PCR data and the recipient STC data, performs a predetermined calculation based on the difference and the host STC data, and sets the calculation result in the host STC counter as the correction data, the PCR data and the recipient STC data being supplied as the variation information data.

35. The host device according to Claim 34, wherein the STC correcting unit calculates a difference by subtracting the recipient STC data from the PCR data, performs the calculation by adding the difference to the host STC data, and sets the calculation result in the host STC counter as the correction data, the PCR data and the recipient STC data being supplied as the variation information data.

36. The host device according to Claim 33, wherein the STC correcting unit obtains a difference between the PCR data and the recipient STC data, performs a predetermined calculation based on the difference and the host STC data, and sets the calculation result in the host STC counter as the correction data, the difference between the PCR data and the recipient STC data being supplied as the variation information data.

37. The host device according to Claim 36, wherein the STC correcting unit obtains a difference by subtracting the recipient STC data from the PCR data, performs the calculation by adding the difference to the host STC data, and sets the calculation result in the host STC counter as the correction data, the difference by subtracting the recipient STC data from the PCR data being supplied as the variation information data.

38. The host device according to any one of Claims 34 through 37, wherein the variation information data is transmitted from the digital signal receiving device to the host device via the interface section while being attached to the stream signal.

39. The host device according to Claim 38, wherein the host device is connectable with the digital signal receiving device via a digital interface in such a manner that at least the stream signal, the clock signal, and the variation information data sent from the digital signal receiving device are receivable in the host device via the digital interface.

40. The host device according to Claim 39, wherein the host device is configured such that at least the stream signal, the clock signal, and the variation information data sent from the digital signal receiving device formed as an electronic card are receivable.

41. The host device according to Claim 40, wherein the electronic card is configured as an SD card.

42. The host device according to Claim 41, wherein the host device receives at least the stream signal, the clock signal, and the variation information data through a data line defined in compliance with the specification of the SD card.

43. The host device according to Claim 42, wherein the host device includes a command sending unit which sends, to the digital signal receiving device, command data for controlling the respective processing in the digital signal receiving device, and a notification receiving unit which receives information from the digital signal receiving device.

44. A semiconductor integrated circuit for producing a host device which is adapted to receive a stream signal and a clock signal from a digital signal receiving device via an interface section in a digital signal receiving system configured such that the host device and the digital signal receiving device are interconnected with each other via the interface section, the digital signal receiving device being adapted to receive a digital communication signal, having a function of generating the clock signal based on PCR data included in the communication signal, and having a function of sending the stream signal in the form of a plurality of packets, as well as the clock signal, the semiconductor integrated circuit being adapted to produce the host device which is connectable with the digital signal receiving device comprising: a recipient STC counter which counts the number of clocks of the clock signal, and outputs the counter value as recipient STC data; a variation detector which calculates a difference between the recipient STC data and the PCR data as

difference data, and detects a variation in frequency of the clock signal that exceeds a predetermined value based on the difference data; and a variation processor which sends, to the host device, variation information data obtained based on the recipient STC data and the PCR data, and sets the PCR data in the recipient STC counter if the variation detector detects that the variation in frequency that exceeds the predetermined value, the semiconductor integrated circuit comprising:

a host STC counter which counts the number of clocks of the clock signal sent from the digital signal receiving device, and outputs the counter value as host STC data; and

an STC correcting unit which calculates correction data based on the host STC data and the variation information data if the variation detector detects the variation in frequency that exceeds the predetermined value, and sets the correction data in the host STC counter so as to coincide the counter value set in the recipient STC counter with the counter value set in the host STC counter.

45. The semiconductor integrated circuit according to Claim 44, further comprising an interface unit provided in the host device for receiving the stream signal, the clock signal, and the variation information data from the digital signal receiving device.

46. The semiconductor integrated circuit according to

Claim 44 or 45, further comprising a decoder for decoding the stream signal and outputting the decoded signal.

47. The semiconductor integrated circuit according to any one of Claims 44 through 46, further comprising a controlling unit which controls respective units in the host device, and generates and outputs command information indicative of commands to respective units in the digital signal receiving device.